In the claims:

For the Examiner's convenience all pending claims are presented herein. Claims that are unchanged are identified as "unchanged":

1. (Amended) A [system to test a bus, the] system comprising:

[at least one] instruction memory to store a plurality of predefined bus stimuli [instruction] instructions, the predefined bus stimuli [instruction] instructions representing a plurality of bus [transaction] transactions; and

[at least one] one or more phase [generator] generators coupled between [the] a bus and the instruction memory, the [at least] one or more phase [generator] generators to [provide] drive signals [to] on the bus corresponding to [the bus transaction in response to] the predefined bus stimuli [instruction] instructions.

2. Cancel

3. (Amended) The system of claim 1, wherein the [instruction comprises an] instructions comprise instruction [word] words having a predefined length.

4. (Amended) The system of claim 1, wherein the [at least one phase generator is] one or more phase generators are further responsive to signals received from the bus.

5. (Amended) The system of claim [2] 1, further comprising a response memory coupled to the phase generator storing predefined responses to signals received from the bus.

6. (Amended) The system of claim 1, wherein the at least one of the one or more phase [generator] generators includes at least one digital logic device responsive to the instructions and at least one phase engine for controlling timing of the bus stimuli.

7. (Unchanged) The system of claim 6, wherein the digital logic device comprises a field programmable gate array.

8. (Unchanged) The system of claim 6, wherein the digital logic device comprises an application specific integrated circuit.

9. (Unchanged) The system of claim 6, wherein the at least one digital logic device includes a control portion for providing bus control signals and a data portion for sending data to the bus.

10. (Unchanged) The system of claim 9, wherein the control portion includes a flow logic device, a request logic device, and a data logic device.

11. (Unchanged) The system of claim 6, wherein the at least one phase engine includes at least one logic level translation device.

12. (Unchanged) The system of claim 6, wherein the at least one phase engine comprises a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine.

13. (Unchanged) The system of claim 9, further comprising a data memory coupled to the data portion.

14. (Unchanged) The system of claim 9, wherein the data portion further receives data from the bus.

15. (Amended) A [system to test a bus, the] system comprising:

an instruction memory for storing [digital data representing] a predefined sequence of bus stimuli representing a plurality of bus transactions;

a flow logic device responsive to the instruction memory;

a request logic device responsive to the instruction memory;

a data logic device responsive to the instruction memory;

a data memory coupled to the data logic device for storing data to be exchanged with agents on [the] a bus;

a system protocol generator coupled to the bus and the flow logic device;

an arbitration protocol generator coupled to the flow logic device and the bus;

a request protocol generator coupled to the flow logic device, the request logic device and the bus;

a snoop/error protocol generator coupled to the request logic device and the bus;

a data protocol engine coupled to the data logic device; and

a transaction response memory coupled to the flow logic device and the request logic device storing digital data representing predefined responses to signals received from the bus.

16. (Amended) A system [to test a bus, the system] comprising:

a first means for storing instructions representing a plurality of predefined bus transactions [stimuli]; and

second means for [providing] driving the plurality of predefined bus transactions as signals [to] on the bus [in response to the stored instructions].

17. (Unchanged) The system of claim 16, further comprising third means for storing data representing predefined responses to signals received from the bus, and wherein the second means implements the predefined responses based on the signals received from the bus.

18. (Unchanged) The system of claim 16, further comprising fourth means for controlling the timing of the signals provided to the bus by the second means.

19. (Unchanged) The system of claim 16, further comprising fifth means for storing data to be exchanged with agents on the bus, wherein the second means transmits data from the fifth means in response to the instructions stored in the first means.

20. (Unchanged) The system of claim 19, wherein the second means further receives data from the bus and stores the data in the fifth means.

21. A method for testing a bus comprising:

receiving instruction words [representing] corresponding to predefined bus stimuli, the predefined bus stimuli representing a plurality of bus transactions; and

executing the plurality of bus transactions by converting the instruction words to signals and driving the signals on the bus [that, when applied to the bus, execute at least one phase of a bus transaction].

22. (Amended) The method of claim 21, further comprising the acts of:

defining a sequence of desired bus transactions; and

assembling the sequence of desired bus transactions into [an object file comprising] instruction words [representing predefined bus stimuli

that, when applied to a bus, implement the sequence of bus transactions], wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus .

23. (Amended) The method of claim 21, further comprising [the act of] providing predefined signals to the bus in response to signals received from the bus.

24. (Amended) The method of claim 21, further comprising [the act of] exchanging data with agents on the bus.

25-28: Cancel

29. (Amended) A system [to test a bus] comprising:

[at least one] an instruction memory to store a plurality of predefined bus stimuli [instruction] instructions, the predefined bus stimuli [instruction] instructions representing signals associated with a plurality of bus [transaction] transactions on [the] a bus;

at least one phase generator coupled between the bus and the instruction memory, the at least one phase generator to provide signals to the bus corresponding [in response] to the predefined bus stimuli [instruction] instructions.

30. (Amended) The system of claim 29, wherein the predefined bus stimuli [instruction] instructions also [represents] include the manner in which the signals are to be transmitted.

Please add the following new claims:

31. a method comprising:

generating a plurality of instructions words corresponding to a predefined sequence of bus transactions;

storing the instructions words in a memory; and

executing the bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence.

32. The system of claim 1, further comprising:

an interface other than the bus coupled to the instruction memory, the interface for connection with a device to receive a plurality of predefined bus stimuli instructions.

33. The system of claim 1, wherein the plurality of predefined bus stimuli instructions are configured as to drive a predefined ordered sequence of bus transactions onto the bus.